REMARKS

By this amendment, claims 1, 6, 7, and 14 have been amended. Accordingly, claims 1-18 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. The specification has been amended to update the priority data and to correct typographical errors. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Rejections Under the Judicially Created Doctrine of Double Patenting

Claims 1-5 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-9 of U.S. Patent No. 6,107,686 to Sandhu et al. (hereinafter "*Sandhu*") for the reasons set forth on page 5 of the Office Action. Claims 6-18 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-9 of *Sandhu* in view of U.S. Patent No. 5,708,303 to Jeng (hereinafter "*Jeng* '303") for the reasons set forth on pages 5-6 of the Office Action.

These rejections will be addressed when allowable subject mater has been indicated by the Examiner.

2. Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1, 3-9, 11-14, and 16-18 have been rejected under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being obvious over *Jeng* '303 for the reasons set [illegible] 2-3 of the Office Action. Applicants respectfully traverse

plurality of lines are comprised of a "single" conductive material. Such a structure is simpler, has

less elements, and requires less fabrication than the structures taught by *Jeng* '303. In particular, *Jeng* '303 discloses interconnect leads composed of a metal barrier layer 62, a metal layer 58, and a metal cap layer 60. As seen in Figures 17-18 of *Jeng* '303, dielectric layer 64 contacts layers 60 and 62, but does not contact the upper or lower surfaces of metal layer 58. In contrast, the upper and lower surfaces of the single conductive material of each line as recited in present claim 1 contact the respective one of the first and second dielectric layers. Thus, the presently recited structure of claim 1 provides a simpler design over *Jeng* '303 while continuing to provide the advantage of reduced capacitance.

With regard to independent claim 6 and dependent claims 7-9 and 11-13, Applicants note that present claim 6 recites: "the lower surfaces of each line of said plurality of lines is in contact with said upper surface of said first dielectric layer." This structure is simpler, has less elements, and requires less fabrication than the structures taught by *Jeng* '303, which include a barrier layer 62 below metal layer 58. As a result, the lower surface of metal layer 58 in *Jeng* '303 does not contact an underlying dielectric layer because of the barrier layer 62. Thus, the presently recited structure of claim 6 provides a simpler design over *Jeng* '303 while continuing to provide the advantage of reduced capacitance.

With regard to independent claim 14 and dependent claims 7 and 16-18, claims 7 and 14 have been amended to recite that each of the plurality of lines has at least one side surface and that "at least one side surface of the dielectric material is (being) in contact with at least one side surface of at least one of the plurality of lines." Present claim 14 further recites a silicon dioxide layer over a [illegible] with the silicon dioxide layer "not being in contact with at least one side

application as filed on page 14, lines 3-4. Such a feature allows [illegible]

dielectric material" to be "in contact with at least one side surface of at least one of the plurality of lines" as recited in claim 14.

In contrast, as illustrated in Figure 1, *Jeng* '303 discloses a silicon dioxide layer 56 as a liner surrounding the upper and side surfaces of the interconnect leads 58, 60, 62, preventing the low-k material 64 from contacting the side surface of the leads. In addition to being a more complex structure than the one presently recited, the *Jeng '303* structure has the disadvantage of the relatively higher dielectric constant silicon dioxide being interdisposed between lines. This design is less efficient and enables less device miniaturization than having solely low dielectric constant materials between lines.

Claims 2, 10, and 15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 in view of U.S. Patent No. 5,486,493 to Jeng (hereinafter "*Jeng* '493") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Claims 2, 10, and 15 depend from claims 1, 6, and 14, respectively, and thus include the limitations thereof, including the specific limitations discussed hereinabove with respect to the rejections over *Jeng* '303. In addition to being absent from *Jeng* '303, such limitations are also not taught or suggested in *Jeng* '493. Thus, even if the cited references are combined as suggested by the Examiner, not all of the claim limitations are met.

Claims 4, 12, and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 in view of U.S. Patent No. 5,420,075 to Homma et al. (hereinafter "*Homma*") for the reasons set forth on page 4 of the Office Action. Applicants respectfully traverse.

Claims 4, 12, and 17 depend from claims 1, 6, and 14, respectively, and thus include the

over *Jeng* '303. In addition to being absent from *Jeng* '303, such limitations are also not taught or

suggested in *Homma*. Thus, even if the cited references are combined as suggested by the Examiner, not all of the claim limitations are met.

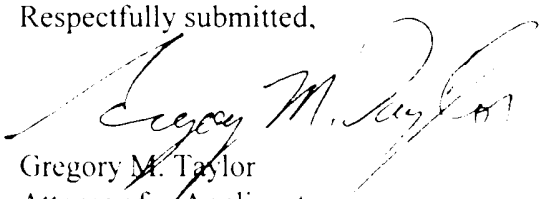
Accordingly, for at least the above reasons, claims 1-18 are not anticipated by or obvious over the cited references. Applicants therefore respectfully request that the rejections of the claims under 35 U.S.C. § 102(e) and/or § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 28th day of February 2002.

Respectfully submitted,



Gregory M. Taylor
Attorney for Applicants
Registration No. 34,263

WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Fax: (801) 328-1707

VERSION WITH MARKINGS SHOWING THE CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 2, line 2 has been amended as follows:

This application is a divisional application of United States Patent Application Serial No. 08/677,514 [677,514], filed on July 10, 1996, now United States Patent No. 6,107,183, which is incorporated herein by reference.

The paragraph beginning at page 3, line 6 has been amended as follows:

One way to decrease unneeded capacitance between metal lines in an integrated circuit is to decrease the dielectric constant of the material between them. Silicon dioxide, the material of choice for interlevel dielectrics, has a relatively high dielectric constant. Replacing silicon dioxide with a material having a lower dielectric constant would thus provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to reliably protect the metal lines, and are unable to withstand further processing.

The paragraph beginning at page 3, line 13 has been amended as follows:

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrated [integrate] circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing dielectric material 18 to processing agents.

The paragraph beginning at page 5, line 2 has been amended as follows:

surface of the dielectric material extending lower than the lower surface of lines 16,

conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of lines of conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing.

IN THE CLAIMS:

Claims 1, 6, 7, and 14 have been amended as follows:

1. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a single conductive material extending along said upper surface of said first dielectric layer, each line of said plurality of lines having upper and lower surfaces, and adjacent lines of said plurality of lines having spaces situated therebetween, the lower surfaces of each line of said plurality of lines being in contact with said upper surface of said first dielectric layer;

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and

a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

6. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a conductive material extending along said upper surface of said first dielectric layer; wherein:

each line of said plurality of lines has an [both a] upper surface, [and] a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

the lower surfaces of each line of said plurality of lines is in contact with said [illegible] first dielectric layer; and

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and

a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

7. (Once Amended) The interlevel dielectric structure as defined in Claim 6, wherein:

said layer of refractory metal nitride has an electrical insulation layer thereon, said electrical insulation layer having thereon said second dielectric layer; and

at least one side surface of the dielectric material is in contact with at least one side surface of at least one of the plurality of lines.

14. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a conductive material extending along said upper surface of said first dielectric layer; wherein:

each line of said plurality of lines has an [both a] upper surface, [and] a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

the lower surfaces of each line of said plurality of lines is in contact with said upper surface of said first dielectric layer;

the upper surface of at least one line of said plurality of lines has thereon a layer of titanium nitride;

said layer of titanium nitride has thereon a silicon dioxide layer;

said silicon dioxide layer not being in contact with at least one side surface of at least one of the plurality of lines [has thereon said second dielectric layer];

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the silicon dioxide layer [the upper surface] of each line of said plurality of lines; and

a dielectric material, having at least one side surface, situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines, and at least one side surface of the dielectric material being in contact with at least one